

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	SOI and dimpling	US-PGPUB; USPAT	OR	ON	2005/01/12 11:01
L2	67	SOI and dimple	US-PGPUB; USPAT	OR	ON	2005/01/12 12:49
L3	3995	SOI same (etch or etching)	US-PGPUB; USPAT	OR	ON	2005/01/12 11:25
L4	588	3 and (grind or grinding)	US-PGPUB; USPAT	OR	ON	2005/01/12 11:25
L5	548	4 and @ad<"20030916"	US-PGPUB; USPAT	OR	ON	2005/01/12 12:49
L7	80	SOI same concave	US-PGPUB; USPAT	OR	ON	2005/01/12 12:49
L8	75	7 and @ad<"20030916"	US-PGPUB; USPAT	OR	ON	2005/01/12 12:51
L9	3327	dimple and substrate and @ad<"20030916"	US-PGPUB; USPAT	OR	ON	2005/01/12 12:52
L10	324	9 and (beam same electrons)	US-PGPUB; USPAT	OR	ON	2005/01/12 12:52
L11	200	10 and (silicon same substrate)	US-PGPUB; USPAT	OR	ON	2005/01/12 13:00
L12	15	(silicon adj on adj insulator)	US-PGPUB; USPAT	OR	ON	2005/01/12 13:01
L13	14756	SOI and @ad<"20030916"	US-PGPUB; USPAT	OR	ON	2005/01/12 13:02
L14	184	13 and HF and TMAH	US-PGPUB; USPAT	OR	ON	2005/01/12 13:36
L15	2	(passive with voltage with contrast) and (SOI or (silicon adj on adj insulator))	US-PGPUB; USPAT	OR	ON	2005/01/12 13:37
L16	0	(passive with voltage with contrast) and (SOI or (silicon adj on adj insulator))	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/12 13:37

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	7	passive adj voltage adj contrast	US-PGPUB; USPAT	OR	ON	2005/01/12 14:06
L2	3	passive adj voltage adj contrast	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/12 14:06

US-PAT-NO: 6812050

DOCUMENT-IDENTIFIER: US 6812050 B1

TITLE: System and method of evaluating gate oxide integrity for semiconductor microchips

----- KWIC -----

Abstract Text - ABTX (1):

The present invention provides a system and method for evaluating gate oxide integrity in a semiconductor wafer. The system may include: a semiconductor wafer; a layer of gate oxide on the semiconductor wafer; a layer of polysilicon on the gate oxide; an electron beam microscope with adjustable energy levels, wherein the electron beam is directed at the semiconductor wafer; an electron beam inspection tool used to detect passive voltage contrasts within the gate oxide layer. The system may also include a measuring tool for measuring an electrical current level of the semiconductor substrate. The system may also include an electrical ground connected to the semiconductor wafer. The system may also include the energy levels vary from about 600 eV to 5000 eV.

Detailed Description Text - DETX (7):

Electron-beam (e-beam) tools like the Secondary Electron Microscopes (SEM) and E-beam inspection tools like eS20 (Registered TM of KLA-Tencor Corporation) are regularly used for imaging defects (SEM) and detecting passive voltage contrast (eS20). The tools employ an electron beam with adjustable beam energies. Now referring to FIGS. 2 and 3, the e-beam 100, when incident on a wafer 101, induces secondary electrons 102 which are produced due to interaction of e-beam electrons with the surface atoms of the wafer, including the gate oxide 106 on top of a silicon wafer substrate 108. The emitted secondary electrons 102 are then captured by a secondary electron detector (not shown) to image the wafer 101 surface. A ground path that leads to the surface of wafer 101 conducts electrons away from the wafer surface as shown in the general direction by arrow 104.

Detailed Description Text - DETX (9):

In addition, poly features 120 which are not grounded or have a presence of an insulating dielectric 106 between them and the wafer substrate 108, result in charge accumulation on the surface. The charge accumulation builds up an electrical field across the dielectric oxide. These features appear bright to the secondary electron detector as the surface accumulates charge. These bright and dark contrasts are termed 'passive voltage contrast'. A dark feature indicates catastrophic breakdown in the gate oxide integrity. SEM inspection tools like the eS20 can be programmed to detect such voltage contrast differences. For thin gate oxides, such an electrical field resulting from incident e-beams will stress the oxide and induce a 'stress induced leakage current' (SILC). SILC is analogous to current voltage characteristics

obtained at the end of line on a finished product probe yield. With increasing electrical fields, the dielectric eventually breaks down and bleeds charge to the wafer substrate. This is effectively gate oxide breakdown. The breakdown changes the charge density on the feature surface and its secondary electron scattering intensity changes from 'bright' to 'dark'. Essentially, gate oxides under poly features which are weaker will leak and breakdown at lower e-beam energies and lesser charge accumulation fields than more robust oxides. A soft breakdown can be detected as a relative increase in substrate current from nominal value for a known oxide thickness through the same methods. Thus, a tool like the eS20 can then be used to identify regions of weak oxides which change contrast for lower e-beam energies due to breakdown. This system and method can be implemented by successively scanning the wafers to detect voltage contrast with successive ramped e-beam energies. In the one embodiment, substrate currents were measured for e-beams with increasing energies between 600 [v] eV and 5000 [v] eV. The charge needed to breakdown is used to extract a spatial GOI metric.

Claims Text - CLTX (7):

7. The method of claim 1 further including using the electron beam inspection tool to detect passive voltage contrasts within a gate structure.

Claims Text - CLTX (8):

8. A method for evaluating gate oxide integrity within a transistor in a semiconductor wafer, the method comprising: providing a semiconductor wafer; forming a gate oxide layer of 0 to 100 angstroms on the semiconductor wafer; forming a polysilicon layer on the gate oxide layer; directing an electron beam of variable energy toward the semiconductor wafer; using an electron beam inspection tool to measure passive voltage contrasts within the gate oxide layer, and estimating and mapping a thickness of the gate oxide layer.

US-PAT-NO: 6236222

DOCUMENT-IDENTIFIER: US 6236222 B1

TITLE: Method and apparatus for detecting misalignments in  
interconnect structures

----- KWIC -----

Abstract Text - ABTX (1):

Disclosed is a method for inspecting electrical interconnections in a multi-level semiconductor device. The method includes forming an interconnect structure in the multi-level semiconductor device. The interconnect structure has a lower metallization layer that lies in a lower level and an upper metallization layer that lies in an upper level. The method includes performing a passive voltage contrast operation using a scanning electron microscope to produce an image of the upper metallization layer of the interconnect structure. The method further includes inspecting the image produced by the scanning electron microscope to determine whether a misalignment is present in the interconnect structure. Additionally, the scanning electron microscope applies a beam of electrons over a selected portion of the interconnect structure, and secondary electrons are emitted off of the upper metallization layer in response to the beam of electrons. Therefore, by examining the intensity levels of the secondary electrons, it is possible to determine whether misalignments have occurred.

Brief Summary Text - BSTX (16):

In one embodiment, a method for inspecting electrical interconnections in a multi-level semiconductor device is disclosed. The method includes forming an interconnect structure in the multi-level semiconductor device. The interconnect structure has a lower metallization layer that lies in a lower level and an upper metallization layer that lies in an upper level. The method includes performing a passive voltage contrast operation using a scanning electron microscope to produce an image of the upper metallization layer of the interconnect structure. The method further includes inspecting the image produced by the scanning electron microscope to determine whether a misalignment is present in the interconnect structure.

Brief Summary Text - BSTX (18):

In yet another embodiment, a system for inspecting electrical interconnections in an interconnect structure of a multi-level semiconductor device is disclosed. The interconnect structure has a lower metallization layer that lies in a lower level and an upper metallization layer that lies in an upper level. The system includes a means for performing a passive voltage contrast operation using a scanning electron microscope to produce an image of the upper metallization layer in interconnect structure. The system further includes a means for inspecting the image produced by the scanning electron

microscope to determine whether a misalignment is present in the interconnect structure.

Drawing Description Text - DRTX (4):

FIG. 2 is a simplified diagram of a passive voltage contrast (PVC) system that may be used for detecting misalignments in interconnect structures in accordance with one embodiment of the present invention.

Detailed Description Text - DETX (3):

FIG. 2 is a simplified diagram of a passive voltage contrast (PVC) system 200 that may be used for detecting misalignments in interconnect structures in accordance with one embodiment of the present invention. As shown, the PVC system includes a vacuum chamber 202 of a scanning electron microscope (SEM) in which a test wafer 206 is placed. Specifically, the wafer 206 rests on a stage 204 within the vacuum chamber 202. The stage 204 includes a wafer support member 212 and a pivoting mechanism 214 for adjusting the angle of the wafer support member 212.

Claims Text - CLTX (3):

performing a passive voltage contrast operation using a scanning electron microscope to produce an electron intensity image that is defined from the upper metallization layer of the interconnect structure; and

Claims Text - CLTX (18):

13. A method for inspecting electrical interconnections in a semiconductor device as recited in claim 1, wherein a computer system is coupled to the scanning electron microscope that is set to repetitively perform the passive voltage contrast operation and the inspecting operation over a wafer.

Claims Text - CLTX (26):

means for performing a passive voltage contrast operation using a scanning electron microscope to produce an electron intensity image that is defined from the upper metallization layer in interconnect structure; and

US-PAT-NO: 6777312

DOCUMENT-IDENTIFIER: US 6777312 B2

TITLE: Wafer-level transfer of membranes in semiconductor processing

----- KWIC -----

Detailed Description Text - DETX (4):

Referring to FIG. 1A, the carrier wafer 100 is a silicon-on-insulator (SOI) wafer which includes the silicon membrane 101 (e.g. on the order of one micron to tens of microns), a thick single-crystal silicon layer 105 (e.g., a few hundred microns), and a thin insulator layer 103 of less than one micron formed of an insulating material such as a silicon oxide and a silicon nitride and sandwiched between the silicon layers 101 and 105. The insulator layer 103 is assumed to be silicon dioxide as an example in the following description. A semiconductor other than silicon may be used for the wafers 100 and 200, including germanium, a III-V compound like GaAs and GaP, and a II-VI compound. The use of GaAs and other semiconductors for semiconductor opto-electronic devices as the device wafer 200 allows for integration opto-electronic components in the final device.

Detailed Description Text - DETX (9):

The selective etching is performed in 3 etching steps. First, the bulk of the silicon in the central region 220 of the silicon layer 105 is etched away by a wet etching process which may be performed by exposing the central region 220 of the silicon layer 105 in a 25 wt % Tetramethylammonium hydroxide (TMAH) bath at about 80.degree. C. until the buried oxide layer 103 is exposed. Other etching chemicals such as KOH may also be used in the wet etching process. This produces a central opening 301 in the carrier wafer 100 and leaves the peripheral portion 302 unchanged due to the isolation by the Teflon fixture (FIG. 3B). Second, the exposed insulator layer 103, i.e., the oxide layer in this example, is removed by first an ashing process by using an oxygen plasma in a plasma etching chamber to remove a bulk part and then by using dilute hydrofluoric acid (49% HF) droplets to remove the residual oxide. This process exposes the membrane 101 in the opening 301 (FIG. 3C).

Detailed Description Text - DETX (13):

FIGS. 6A-6L illustrate fabrication of a deformable mirror where both the mirror and the underlying actuators are fabricated by the membrane transfer process. FIG. 6A shows a SOI carrier wafer and silicon device wafer are prepared. In FIG. 6B, a 1-micron thick corrugated polysilicon membrane is fabricated on the SOI wafer and is doped to be conductive as part of an electrostatic actuator array on the device wafer that deform the mirror. The corrugated structure is designed to control the deflection of the actuator and to release the stress caused by the bonding and deposition process and the

intrinsic stress of membrane materials.

Detailed Description Text - DETX (16):

FIGS. 8A-8D show fabrication of another deformable mirror where a reflective silicon membrane 101 in a SOI carrier wafer is directly transferred onto an array of actuators 810 formed on a device wafer 800. The actuators 810 may be previously fabricated on the wafer 800.

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#### 1 Identification of processing defects by focused ion beam (FIB) induced voltage contrast

*Chun-Sheng Liu; Chih-Rong Chen; Yong-Fen Hsieh;*

Physical and Failure Analysis of Integrated Circuits, 1999. Proceedings of the 7th International Symposium on the , 5-9 July 1999

Pages:128 - 131

[\[Abstract\]](#)    [\[PDF Full-Text \(572 KB\)\]](#)    IEEE CNF

#### 2 Failure analysis for the 0.13 $\mu\text{m}$ Cu/low k (Black Diamond/trade/) interconnection by the passive voltage contrast

*Li Hongyu; Su Yong Jie; Tsang Chi Fo; Patrick, Y.W.C.; Koh Mei Ling; Wong Li Tang Leijun; Li Wei Hong; Chang Chang Kuo; Bliznetsov, V.; Lin, Z.;*

Electronics Packaging Technology, 2003 5th Conference (EPTC 2003) , 10-12 2003

Pages:342 - 345

[\[Abstract\]](#)    [\[PDF Full-Text \(296 KB\)\]](#)    IEEE CNF

#### 3 Front-end processing defect localization by contact-level passive voltage contrast technique and root cause analysis

*Song, Z.G.; Dai, J.Y.; Ansari, S.; Oh, C.K.; Redkar, S.;*

Physical and Failure Analysis of Integrated Circuits, 2002. IPFA 2002. Proceedings of the 9th International Symposium on the , 8-12 July 2002

Pages:97 - 100

[\[Abstract\]](#)    [\[PDF Full-Text \(872 KB\)\]](#)    IEEE CNF

#### 4 Application of contact-level ion-beam induced passive voltage contrast failure analysis of static random access memory

*Song, Z.G.; Qian, G.; Dai, J.Y.; Guo, Z.R.; Loh, S.K.; Teh, C.S.; Redkar, S.;*  
Physical and Failure Analysis of Integrated Circuits, 2001. IPFA 2001. Proceed  
of the 2001 8th International Symposium on the , 9-13 July 2001  
Pages:103 - 106

[\[Abstract\]](#) [\[PDF Full-Text \(1032 KB\)\]](#) IEEE CNF

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**5 Application of passive voltage contrast and focused ion beam on fail analysis of metal via defect in wafer fabrication**

*Ang, G.B.; Hua, Y.N.; Loh, S.K.; Yogaspari; Redkar, S.;*  
Physical and Failure Analysis of Integrated Circuits, 2001. IPFA 2001. Proceed  
of the 2001 8th International Symposium on the , 9-13 July 2001  
Pages:107 - 111

[\[Abstract\]](#) [\[PDF Full-Text \(1400 KB\)\]](#) IEEE CNF

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**6 Finding voids in dual damascene Cu vias and their impact on reliabil**  
*Dong, W.; Ji, J.; Sanan Liang; Zhang, M.; Liao, S.; Chorong Niou; Wei-Ting Ka;*  
*Chien;*

Reliability Physics Symposium Proceedings, 2004. 42nd Annual. 2004 IEEE  
International , 25-29 April 2004  
Pages:343 - 346

[\[Abstract\]](#) [\[PDF Full-Text \(389 KB\)\]](#) IEEE CNF

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**7 Failure rate and yield-limiting tungsten plug corrosion diagnosis usi**  
**characterization test vehicles**

*Xing Tao; Reis, K.; Haby, B.; Karnett, M.; White, N.; Watts, C.; Delgado, M.;*  
*Gardner, K.; Harris, K.R.;*  
Advanced Semiconductor Manufacturing 2002 IEEE/SEMI Conference and  
Workshop , 30 April-2 May 2002  
Pages:144 - 149

[\[Abstract\]](#) [\[PDF Full-Text \(657 KB\)\]](#) IEEE CNF

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**8 Poly-residue-induced contact failures in 0.18  $\mu\text{m}$  technology**

*Teh, C.S.; Song, Z.H.; Dai, J.Y.; Guo, Z.R.; Redkar, S.;*  
Physical and Failure Analysis of Integrated Circuits, 2001. IPFA 2001. Proceed  
of the 2001 8th International Symposium on the , 9-13 July 2001  
Pages:117 - 120

[\[Abstract\]](#) [\[PDF Full-Text \(376 KB\)\]](#) IEEE CNF

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**9 Failure mechanism study for high resistance contact in CMOS device**

*Dai, J.Y.; Ansari, S.; Tay, C.L.; Tee, S.F.; Er, E.; Redkar, S.;*  
Physical and Failure Analysis of Integrated Circuits, 2001. IPFA 2001. Proceed  
of the 2001 8th International Symposium on the , 9-13 July 2001  
Pages:130 - 133

[\[Abstract\]](#) [\[PDF Full-Text \(296 KB\)\]](#) IEEE CNF

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**10 Failure analysis from the back side of a die**

*Liebert, S.;*

Physical and Failure Analysis of Integrated Circuits, 2001. IPFA 2001. Proceed of the 2001 8th International Symposium on the , 9-13 July 2001  
Pages:187 - 194

[\[Abstract\]](#) [\[PDF Full-Text \(1784 KB\)\]](#) [IEEE CNF](#)

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**11 Defect isolation and characterization in contact array/chain structure by using voltage contrast effect**

*Sakai, T.; Oda, N.; Yokoyama, T.; Kikuchi, H.; Kitajima, H.;*

Semiconductor Manufacturing Conference Proceedings, 1999 IEEE International Symposium on , 11-13 Oct. 1999

Pages:195 - 198

[\[Abstract\]](#) [\[PDF Full-Text \(208 KB\)\]](#) [IEEE CNF](#)

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**12 Rapid in-line characterization of plasma-induced damage on a 0.25 CMOS ASIC technology**

*Liang, V.; Bothra, S.; Sur, H.; Sengupta, S.;*

Plasma Process-Induced Damage, 1998 3rd International Symposium on , 4-5 1998

Pages:148 - 151

[\[Abstract\]](#) [\[PDF Full-Text \(412 KB\)\]](#) [IEEE CNF](#)

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